Exercise (SS 2022)

Comunication Systems and Protocols

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Task 1: Actuator Sensor Interface (ASI)

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In the following a data transmission on the ASI bus is considered. Thereby a master wants to transmit the bit vector 01001 to the slave having address 26_d. The telegram format of the ASI bus is shown in Figure 1.1.

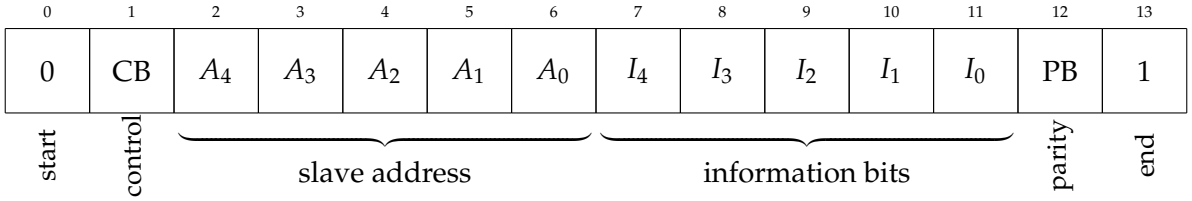

Figure 1.1: ASI packet format, master call

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1.1 Specify the course of the sender voltage on the ASI bus. A time offset does not need to be considered (Note: The control bit must have value '0' for data transmission, use even parity without considering start / stop bits). Use figure 1.2 and Manchester as per IEEE 802.3

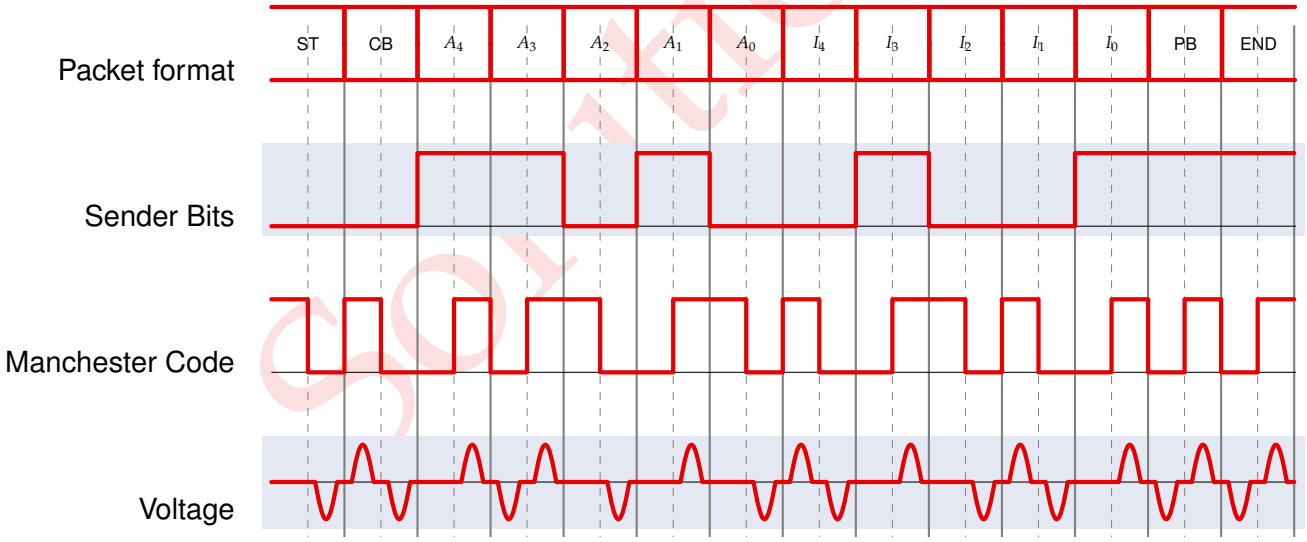

Figure 1.2: Waveform of the sender voltage

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1.2 Figure 1.3 shows the waveform on the ASI bus when transmitting a master call. Due to external influences the transmission has been disturbed. Mark the errors and name the rule(s) by which they are detected.

1. Start and stop bits: first impulse has to be negative, last impulse has to be positive
2. Succeeding impulses must have different polarity
3. Between two impulses of a telegram the pause that is allowed lasts half a bit time at maximum
4. The parity of the telegram must be even. In the example this cannot be seen since the transmitted data cannot be reconstructed due to the great amount of errors

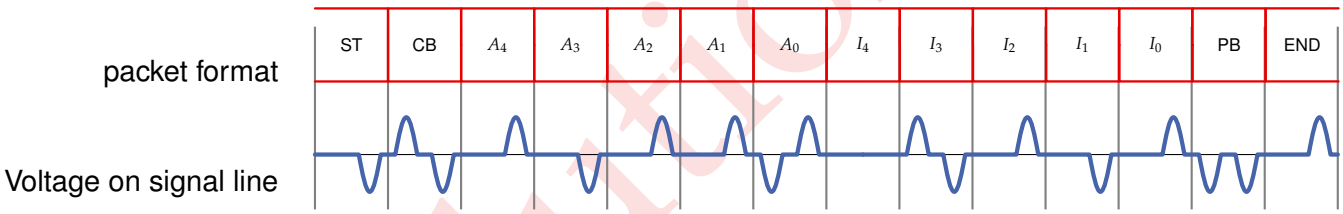

Figure 1.3: Waveform of the sender voltage

Task 2: I²C-Bus Synchronization

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Three I²C Bus Masters want to send data to one slave. Each node needs one time step to read in data from external signal lines (SCL, SDA). The reaction time within each node is negligibly small (0 time steps). The individual masters want to establish a clock signal according to the following table 2.1:

Master	Low period	High period
A	8	4
B	4	12
C	12	8

Table 2.1: clock signals

Assume that Master B is initiating the communication cycle.

2.1 In general, which functionality does the I²C bus provide for the case that multiple master nodes want to communicate at the same time with the same slave node? 1

The I²C-Bus uses clock synchronization and arbitration (over the complete dataframe, over address and data fields).

2.2 Complete the waveforms of the signals that result from the interaction between the nodes on the SCL signal. 3

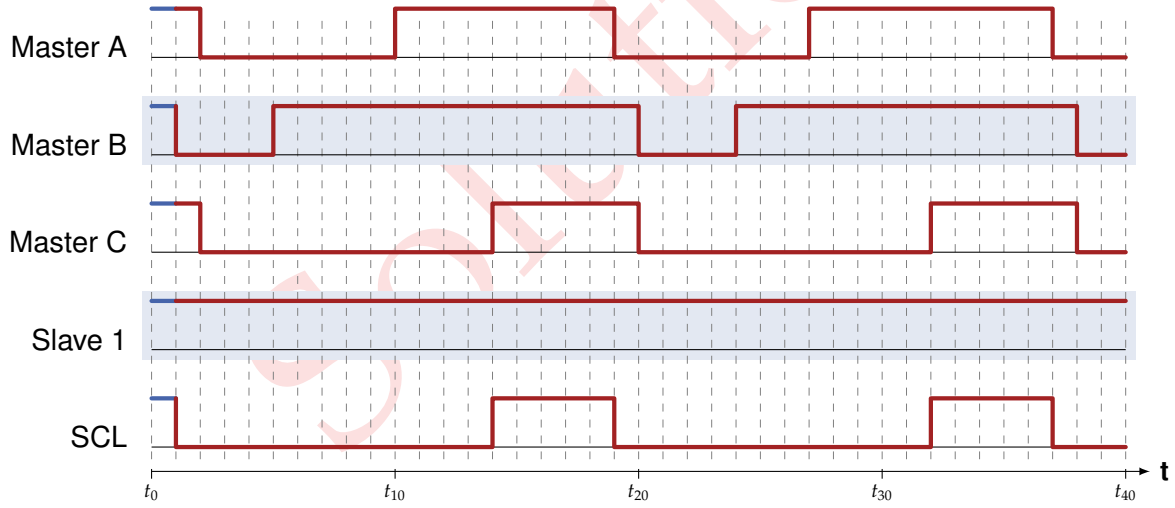

Figure 2.1: Signal sequence

2.3 In general, which functionality does the I2C bus provide for the case when there is a fast and a slow master node? 2

The I²C-Bus allows slower nodes to insert wait states if the other node is too fast. The wait state insertion is controlled by the SCL signal. In general, the SCL signal is generated by a wired-AND connection with dominant "LOW" of the participants CLK signals. A wait state is inserted if the SCL signal remains "LOW" and is initiated by a slower node.

Task 3: FireWire

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3.1 FireWire uses a special coding scheme with an additional STROBE signal. Indicate the impulse diagram for the case that the following bit sequence (given in binary notation) should be transmitted. Use figure 3.1 1

$$100110100011011110111100_b$$

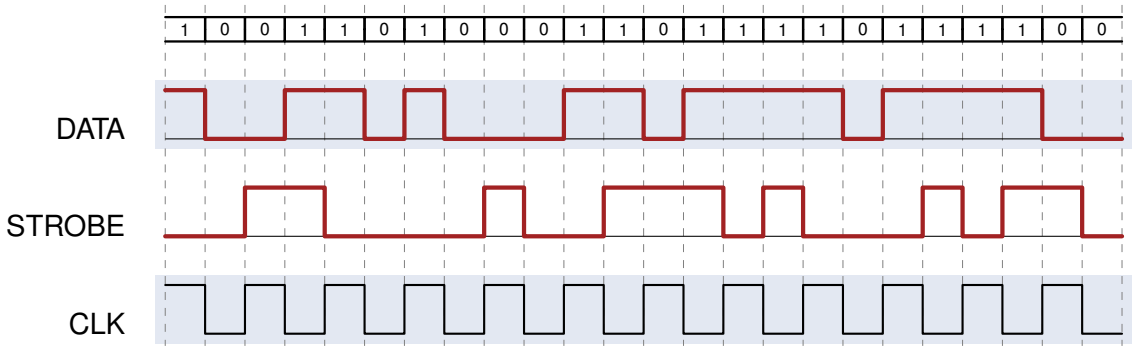

Figure 3.1: FireWire impulse diagram

Several FireWire devices are interconnected as shown in Figure 3.2.

3.2 Perform the three steps of address assignment for this network. Assume that every node needs one time unit for processing and forwarding of a message. Every node can process several incoming messages in parallel. In Figure 3.2 fill in the address that is obtained by every node. Which node becomes root of the tree? 3

The node with the adress 10 is the root of the network.

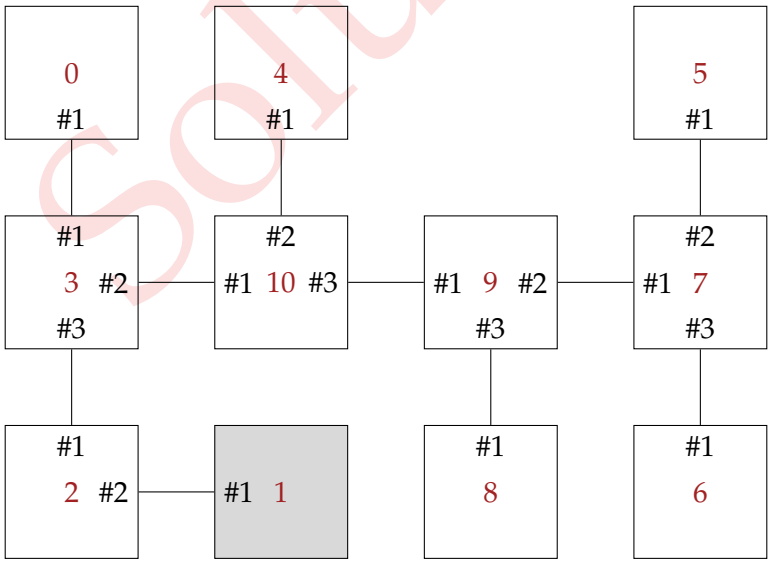

Figure 3.2: FireWire network

3.3 Now assume that the node highlighted in grey is not part of the network any more. What is the problem now during address assignment? 3
How could this problem be solved?

problem: Two nodes sending a parent request at the same time. Which node becomes root?

Solution: Random waiting time for the two remaining participants. After the waiting time a new notification message is transmitted. The participant that needs to wait for a longer time becomes root.

FireWire structures

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3.4 Different FireWire structures were built during a student laboratory. During test phase you notice that not all FireWire systems are working correctly. Please state if the FireWire systems given below are working correct. Mark the roots, if the systems are correct. Give a reason, if the FireWire system is not working correctly.

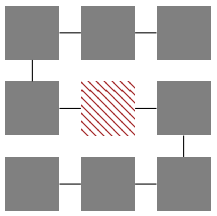
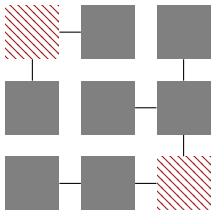
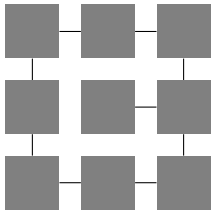
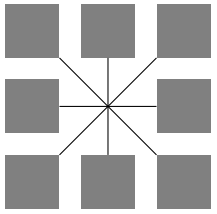
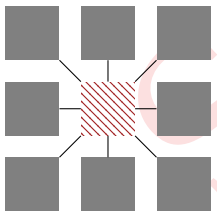
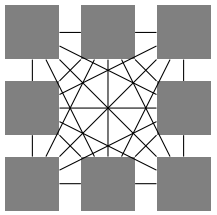
	Correct	Wrong	Reason
	x		
	x		
		x	Rings are not allowed in FireWire
		x	One output cannot have multiple connections
	x		
		x	Rings are note allowed in FireWire

Table 3.1: FireWire structures